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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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	Complete If Known	
Application Number	09/841,974	
Filing Date	4/24/01	
First Named Inventor	Terry Lee Goode	
Art Unit	2128	
Examiner Name	Fred O. Ferris III	•
Attorney Docket Number	003921.00011	

U.S. PATENT DOCUMENTS							
Examiner initials	Cite No.1	Document Number Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant		
17	<u> </u>	US- 5,649,176	07-15-1997	Selvidge, et al.	Figures Appear		
3		US- 5,659,716	08-19-1997	Selvidge, et al.			
~(-		US- 5,841,967	11-24-1998	Sample, et al.			
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niner C	Cite	Foreign Patent Document	Publication	Name of Patentee or	Pages, Columns, Lines,	
	No.1	Country Code ⁵ · Number ⁶ · Kind Code ⁶ (if known)	Date MM-OD-YYYY	Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear	T ⁶
7		JP 1-154251	06-1989			No
		GB 1,444,084	07-28-1976	Cheesman		
		GB 2,182,220	05-07-1987	Austin		
			,			

Signature Considered 6//(0)	Examiner Signature	212	Date Considered	8/7/05	
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Complete if Known

09/841.974

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Application Number

Filing Date

ADDINGS TO STAN A TION INFORMATION DISCLOSURE STATEMENT BY APPLICANT

First Named Inventor Terry Lee Goode 2128 Art Unit

(Use as many sheets as necessary)

Fred O. Ferris III Examiner Name

2 003921.00011 Sheet of Attorney Docket Number

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
Z Z		Kronstadt, et al., "Software Support for the Yorktown Simulation Engine," 19th Design Automation Conference, Paper 7.3, 1982, pp. 60-64	
Z		Koike, et al., "HAL: A High-Speed Logic Simulation Machine," IEEE Design & Test, Oct. 1985, pp. 61-73	
3		Shear, "Tools Help you Retain the Advantages of Using Breadboards in Gate-Array Design," EDN, Mar. 18, 1987, pp. 81-88	
Z		J.W. Babb, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation," Masters Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, Nov. 1993; Also available as MIT/LCS Technical Report TR-686	
ξ		M. Dahl, J. Babb, R. Tessier, S. Hanono, D. Hoki, and A. Agarwal, "Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System," IEEE Workshop on FPGAs for Custom Computing Machines '94 (FCCM '94), Apr. 1994	
3		R. Tessier, J. Babb, M. Dahl, D. Hanono and A. Agarwal, "The Virtual Wires Ernulation System: A Gate-Efficient ASIC Prototyping Environment," ACM Workshop on FPGA's (FPGA '94), Feb. 1994	
3	·	J. Babb, R. Tessier, and A. Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," IEEE Workshop on FPGAs for Custom Computing Machines '93 (FCCM '93), Apr. 1993	
3		IKOS Systems to Acquire Virtual Machine Works; IKOS Systems Mar. 11, 1996	
3 3		R. Goering, "Emulation for the Masses," Electronic Engineering Times, Jan. 1996	
3		J. Babb, R. Tessier, and A. Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," Massachusetts Institute of Technology, Student Workshop on Scalable Computing, August 4, 1993	
3		R. Tessier, J. Babb, M. Dahl, D. Hanono, and D. Hoki, 'The Virtual Wires Emulation System; A Gate-Efficient ASIC Prototyping Environment," MIT Student Workshop on Scalable Computing; July 21-22, 1994	
7		Feng, "A Survey of Interconnection Networks," Computer, Dec. 1981, pp. 12-27	
7.		Chapter 36, "Switching Networks and Traffic Concepts," Reference Data for Radio Engineers, Howard W. Sams & Co., 1981, pp. 36-1 to 36-16	
7		S. Hanono, "Inner View Hardware Debugger: A Logic Analysis Tool for the Virtual Wires Emulation System," Masters Thesis, MIT Department of Electrical Engineering and Computer Science, Jan. 1995; Also available as MIT/LCS Technical Report.	

Examiner Signature	2	12	Date Considered	8(7	105

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